RECEIVED CENTRAL FAX CENTER

AUG 3 1 2006

IN THE CLAIMS:

Kindly replace the claims of record with the following full set of claims:

- 1. 2. (cancelled)
- 3. (previously presented) A high frequency receiver (1), which is provided with a front end comprising a low noise amplifier (2), and which is provided with quadrature mixers (3) coupled to the low noise amplifier (2), characterised in that the low noise amplifier is a quadrature low noise amplifier (2-1, 2-2), characterised in that quadrature paths (I, Q) of the quadrature low noise amplifier (2-1, 2-2) are implemented differentially.
- 4. (original) The high frequency receiver (1) according to claim 3, characterised in that the differential quadrature low noise amplifier (2-1; 2-2) is constructed as a class AB operating circuit.
- 5. (previously presented) The high frequency receiver (1) according to claim 3, wherein the quadrature low noise amplifier (2-1, 2-2) comprises a cascode arrangement of semiconductors (15).
- 6. (previously presented) The high frequency receiver (1) according to claim 5, wherein the semiconductors (15) are of the type MOST.
- 7. (C) A high frequency receiver (1), which is provided with a front end comprising a low noise amplifier (2), and which is provided with quadrature mixers (3) coupled to the low noise amplifier (2), characterised in that the low noise amplifier is a quadrature low

Amendment Serial No. 10/055,388 Docket No. NL010029

noise amplifier (2-1, 2-2), in that the quadrature low noise amplifier (2-1, 2-2) comprises a cascode arrangement of semiconductors (15), and in that across the cascode arrangement of semiconductors (15) there is connected a capacitor (C).

- 8. (Previously presented) A high frequency receiver (1), which is provided with a front end comprising a low noise amplifier (2), and which is provided with quadrature mixers (3) coupled to the low noise amplifier (2), characterised in that the low noise amplifier is a quadrature low noise amplifier (2-1, 2-2), characterised in that the high frequency receiver (1) comprises two quadrature choppers (10-1, 10-2) coupled between respective outputs (4, 5) of the quadrature low noise amplifiers, that include said amplifier and another quadrature low noise amplifier, and respective inputs of the quadrature mixers (3-1, 3-2) whose output is demodulated by a quadrature demodulator.
- 9. (previously presented) The high frequency receiver (1) according to claim 8, wherein the quadrature choppers (10-1, 10-2) and quadrature mixers (3-1, 3-2) are combined to passive quadrature choppers/mixers.
- 10. (cancelled)
- 11. (previously presented) A quadrature low noise amplifier for application in the high frequency receiver (1) according to claim 3.

Amendment Serial No. 10/055,388 Docket No. NL010029

- 12. (previously presented) A method for receiving high frequency signals, comprising: implementing, differentially, quadrature paths of a quadrature low noise amplifier disposed at a front end of a high-frequency receiver; and coupling quadrature mixers to the amplifier.
- 13. (Previously presented) The method of claim 12, wherein the differential quadrature low noise amplifier is constructed as a class AB operating circuit.
- 14. (Previously presented) The method of claim 12, wherein the quadrature low noise amplifier comprises a cascode arrangement of semiconductors.
- 15. (Previously presented) The method of claim 14, wherein the semiconductors are of the type MOST.
- 16. (new) The method of claim 12, wherein the coupled quadrature mixers are in a receive circuit of said receiver.
- 17. (new) The method of claim 16, wherein output of said mixers comprises a signal that has been down-converted by said receive circuit.
- 18. (new) The receiver of claim 3, wherein the coupled quadrature mixers are in a receive circuit of said receiver.

Amendment

Serial No. 10/055,388

Docket No. NL010029

- 19. (new) The receiver of claim 18, wherein output of said mixers comprises a signal that has been down-converted by said receive circuit.
- 20. (new) The receiver of claim 7, wherein said cascode arrangement comprises two parallel legs of said semiconductors, both legs being in parallel with said capacitor.
- 21. (new) The receiver of claim 7, wherein said cascode arrangement comprises a differential cascode arrangement.
- 22. (new) The receiver of claim 8, wherein each of said choppers switches its respective outputs for coupling with the other of said choppers.
- 23. (new) The receiver of claim 8, wherein said choppers switch in-phase and quadrature signals.